|  |  |  |
| --- | --- | --- |
| **Introduction**  The sequence circuits and the sequence networks developed in the previous chapter will now be used for finding out fault current during unsymmetrical faults.  **Three Types of Faults**  **http://nptel.ac.in/courses/108104051/chapter_8/images/sdr5.gif**  **Calculation of fault currents**  Let us make the following assumptions:   * The power system is balanced before the fault occurs such that of the three sequence networks only the positive sequence network is active. Also as the fault occurs, the sequence networks are connected only through the fault location. * The fault current is negligible such that the pre-fault positive sequence voltages are same at all nodes and at the fault location. * All the network resistances and line charging capacitances are negligible. * All loads are passive except the rotating loads which are represented by synchronous machines.   Based on the assumptions stated above, the faulted network will be as shown in Fig. 8.1 where the voltage at the faulted point will be denoted by *Vf*and current in the three faulted phases are *Ifa*, *I fb*and *I fc*.  We shall now discuss how the three sequence networks are connected when the three types of faults discussed above occur.   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image002.jpg |  |   **Fig. 8.1 Representation of a faulted segment.** |
| **Single-Line-to-Ground Fault**  Let a 1LG fault has occurred at node *k*of a network. The faulted segment is then as shown in Fig. 8.2 where it is assumed that phase-a has touched the ground through an impedance *Zf*. Since the system is unloaded before the occurrence of the fault we have   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image004.gif | (8.1) |        |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image006.jpg |   **Fig. 8.2 Representation of 1LG fault.**  Also the phase-a voltage at the fault point is given by   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image008.gif | (8.2) |     From (8.1) we can write   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image010.gif | (8.3) |         Solving (8.3) we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image012.gif | (8.4) |       This implies that the three sequence currents are in series for the 1LG fault. Let us denote the zero, positive and negative sequence Thevenin impedance at the faulted point as *Z kk0* , *Z kk1* and *Z kk2*respectively. Also since the Thevenin voltage at the faulted phase is *Vf*we get three sequence circuits that are similar to the ones shown in Fig. 7.7. We can then write   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image014.gif | (8.5) |         Then from (8.4) and (8.5) we can write   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image016.gif | (8.6) |       Again since   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image018.gif |  |       We get from (8.6)   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image020.gif | (8.7) |       The Thevenin equivalent of the sequence network is shown in Fig. 8.3.   |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image022.jpg |   **Fig. 8.3 Thevenin equivalent of a 1LG fault.**    [**Example 8.1**](javascript:openpopup('examp_8.1.html')) |

# **Line-to-Line Fault**

The faulted segment for an L-L fault is shown in Fig. 8.5 where it is assumed that the fault has occurred at node *k*of the network. In this the phases b and c got shorted through the impedance *Zf*. Since the system is unloaded before the occurrence of the fault we have

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image046.gif | (8.8) |

|  |
| --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image048.jpg |

**Fig. 8.5 Representation of L-L fault.**

Also since phases b and c are shorted we have

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image050.gif | (8.9) |

Therefore from (8.8) and (8.9) we have

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image052.gif | (8.10) |

We can then summarize from (8.10)

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image054.gif | (8.11) |

Therefore no zero sequence current is injected into the network at bus k and hence the zero sequence remains a dead network for an L-L fault. The positive and negative sequence currents are negative of each other.

Now from Fig. 8.5 we get the following expression for the voltage at the faulted point

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image056.gif | (8.12) |

Again

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image058.gif | (8.13) |

Moreover since *I fa0* = *I fb0* = 0 and *I fa1* = - *I fb2*, we can write

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image060.gif | (8.14) |

Therefore combining (8.12) - (8.14) we get

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image062.gif | (8.15) |

Equations (8.12) and (8.15) indicate that the positive and negative sequence networks are in parallel. The sequence network is then as shown in Fig. 8.6. From this network we get

|  |  |
| --- | --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image064.gif | (8.16) |

|  |
| --- |
| http://nptel.ac.in/courses/108104051/chapter_8/images/image066.jpg |

**Fig. 8.6 Thevenin equivalent of an LL fault.**

[**Example 8.2**](javascript:openpopup('examp_8.2.html'))

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Double- Line -to Ground Fault**  The faulted segment for a 2LG fault is shown in Fig. 8.7 where it is assumed that the fault has occurred at node *k*of the network. In this the phases b and c got shorted through the impedance *Zf*to the ground. Since the system is unloaded before the occurrence of the fault we have the same condition as (8.8) for the phase-a current. Therefore   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image088.gif | (8.17) |        |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image090.jpg |   **Fig. 8.7 Representation of 2LG fault.**  Also voltages of phases b and c are given by   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image092.gif | (8.18) |       Therefore   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image094.gif | (8.19) |         We thus get the following two equations from (8.19)   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image096.gif | (8.20) |      |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image098.gif | (8.21) |       Substituting (8.18) and (8.20) in (8.21) and rearranging we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image100.gif | (8.22) |       Also since *I fa*= 0 we have   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image102.gif | (8.23) |       The Thevenin equivalent circuit for 2LG fault is shown in Fig. 8.8. From this figure we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image104.gif | (8.24) |         The zero and negative sequence currents can be obtained using the current divider principle as   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image106.gif | (8.25) |        |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image108.gif | (8.26) |        |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image110.jpg |   **Fig. 8.8 Thevenin equivalent of a 2LG fault.**    [**Example 8.3**](javascript:openpopup('examp_8.3.html')) | | | |
| [http://nptel.ac.in/courses/108104051/ui/images/prev.gif](http://nptel.ac.in/courses/108104051/chapter_8/8_3.html)[http://nptel.ac.in/courses/108104051/ui/images/next.gif](http://nptel.ac.in/courses/108104051/chapter_8/8_5.html) |

**FAULT CURRENT COMPUTATION USING SEQUENCE NETWORKS**

In this section we shall demonstrate the use of sequence networks in the calculation of fault currents using sequence network through some examples.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Example 8.4**  Consider the network shown in Fig. 8.10. The system parameters are given below   |  |  | | --- | --- | | Generator *G*: 50 MVA, 20 kV, *X"* = *X*1 = *X*2 = 20%, *X*0 = 7.5% |  |  |  |  | | --- | --- | | Motor *M*: 40 MVA, 20 kV, *X"* = *X*1 = *X*2 = 20%, *X*0 = 10%, *Xn*= 5% |  |  |  |  | | --- | --- | | Transformer *T*1 : 50 MVA, 20 kV Δ /110 kVY, *X*= 10% |  |  |  |  | | --- | --- | | Transformer *T*2 : 50 MVA, 20 kV Δ /110 kVY, *X*= 10% |  |  |  |  | | --- | --- | | Transmission line: *X*1 = *X*2 = 24.2 Ω , *X*0 = 60.5 Ω |  |   We shall find the fault current for when a (a) 1LG, (b) LL and (c) 2LG fault occurs at bus-2.   |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image144.jpg |   **Fig. 8.10 Radial power system of Example 8.4.**  Let us choose a base in the circuit of the generator. Then the per unit impedances of the generator are:   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image146.gif |  |   The per unit impedances of the two transformers are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image148.gif |  |   The MVA base of the motor is 40, while the base MVA of the total circuit is 50. Therefore the per unit impedances of the motor are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image150.gif |  |   For the transmission line   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image152.gif |  |   Therefore   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image154.gif |  |   Let us neglect the phase shift associated with the Y/ Δ transformers. Then the positive, negative and zero sequence networks are as shown in Figs. 8.11-8.13.   |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image156.jpg |   **Fig. 8.11 Positive sequence network of the power system of Fig. 8.10.**   |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image158.jpg |   **Fig. 8.12 Negative sequence network of the power system of Fig. 8.10.**   |  | | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image160.jpg |   **Fig. 8.13 Zero sequence network of the power system of Fig. 8.10.**  From Figs. 8.11 and 8.12 we get the following *Ybus*matrix for both positive and negative sequences   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image162.gif |  |   Inverting the above matrix we get the following *Zbus*matrix   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image164.gif |  |   Again from Fig. 8.13 we get the following *Ybus*matrix for the zero sequence   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image166.gif |  |   Inverting the above matrix we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image168.gif |  |   Hence for a fault in bus-2, we have the following Thevenin impedances   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image170.gif |  |   Alternatively we find from Figs. 8.11 and 8.12 that   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image172.gif  http://nptel.ac.in/courses/108104051/chapter_8/images/image174.gif |  |   **(a) Single-Line-to-Ground Fault**: Let a bolted 1LG fault occurs at bus-2 when the system is unloaded with bus voltages being 1.0 per unit. Then from (8.7) we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image176.gif  per unit |  |   Also from (8.4) we get   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image178.gif  per unit |  |   Also *I fb*= *I fc*= 0. From (8.5) we get the sequence components of the voltages as   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image180.gif |  |   Therefore the voltages at the faulted bus are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image182.gif |  |   **(b) Line-to-Line Fault** : For a bolted LL fault, we can write from (8.16)   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image184.gif  per unit |  |   Then the fault currents are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image186.gif |  |   Finally the sequence components of bus-2 voltages are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image188.gif |  |   Hence faulted bus voltages are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image190.gif |  |   **(c) Double-Line-to-Ground Fault**: Let us assumes that a bolted 2LG fault occurs at bus-2. Then   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image192.gif |  |   Hence from (8.24) we get the positive sequence current as   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image194.gif  per unit |  |   The zero and negative sequence currents are then computed from (8.25) and (8.26) as   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image196.gif  per unit  http://nptel.ac.in/courses/108104051/chapter_8/images/image198.gif  per unit |  |   Therefore the fault currents flowing in the line are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image200.gif |  |   Furthermore the sequence components of bus-2 voltages are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image202.gif |  |   Therefore voltages at the faulted bus are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image204.gif |  | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Example 8.5**  Let us now assume that a 2LG fault has occurred in bus-4 instead of the one in bus-2. Therefore   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image206.gif |  |   Also we have   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image208.gif |  |   Hence   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image210.gif per unit |  |   Also   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image212.gif  per unit |  |  |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image214.gif  per unit |  |   Therefore the fault currents flowing in the line are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image216.gif |  |   We shall now compute the currents contributed by the generator and the motor to the fault. Let us denote the current flowing to the fault from the generator side by *Ig*, while that flowing from the motor by *Im*. Then from Fig. 8.11 using the current divider principle, the positive sequence currents contributed by the two buses are     |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image218.gif  per unit |  |  |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image220.gif per unit |  |   Similarly from Fig. 8.12, the negative sequence currents are given as   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image222.gif per unit |  |  |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image224.gif per unit |  |   Finally notice from Fig. 8.13 that the zero sequence current flowing from the generator to the fault is 0. Then we have   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image226.gif  http://nptel.ac.in/courses/108104051/chapter_8/images/image228.gif  per unit |  |   Therefore the fault currents flowing from the generator side are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image230.gif |  |   and those flowing from the motor are   |  |  | | --- | --- | | http://nptel.ac.in/courses/108104051/chapter_8/images/image232.gif |  |   It can be easily verified that adding *Ig*and *Im*we get *If*given above. |